REMARKS

The Office Action mailed May 11, 2005 has been received and carefully noted. In addition, the undersigned attorney wishes to thank the Examiner for the interview on the present application and the May 11th Office Action. It is submitted that the amendments made herein and the following remarks are submitted as a full and complete response and support and follow the interview with the Examiner concerning this application and the May 11th Office Action.

In this Amendment, claims 1, 3, 5, 6, 11 and 12 have been amended and new independent claim 23 has been added. Payment for the corresponding additional claim fee is submitted in a credit card payment form submitted with this Amendment. Additionally, a request for a three-month extension of time, an RCE and the appropriate credit card payment form for these further filings are filed concurrently with this Amendment and are filed within the deadline of the three-month statutory period, which is November 11, 2005. Authorization is granted to charge counsel's Deposit Account No. 01-2300, referencing **Attorney Docket No. 024016-00063**, for any additional fees necessary for entry of this Amendment.

Applicant accordingly submits that the amendments made herein and additional claim are fully supported in the Specification and the drawings, as originally filed, and therefore no new matter has been introduced. Accordingly, claims 1, 3, 5, 6, 7, 8, 9, 10, 11, 12 and 23 are pending in the present application and are respectfully submitted for reconsideration.

Dependent claim 3 stands objected to for informalities. As has been discussed, claim 3 has been amended in response to the Examiner's objection and is responsive thereto. The objection is accordingly traversed and reconsideration is requested.

Dependent claims 11 and 12 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. As has been discussed, claims 11 and 12 have been amended in response to the

Examiner's rejections and are responsive thereto. The rejections are accordingly traversed and reconsideration is requested.

Claims 1, 3 and 5-12 stand rejected under 35 U.S.C. § 102(b) as being anticipated by the Kokubo et al. patent (U.S. Patent No. 5,982,208). Claims 1, 3, 5, 6, 11 and 12 have been amended and claim 23 has been added. Dependent claims 8-10 and 12 depend from independent claims 7 and 11, respectively. With respect to the rejections of the claims 1, 3 and 5-12 and insofar as such rejections can be applied to newly added independent claim 23, the rejections are respectfully traversed and reconsideration is requested.

Independent claim 1, as amended, recites a clock multiplication circuit for delivering an output clock signal at a frequency that is a multiple of the frequency of a reference clock signal as inputted, the clock multiplication circuit comprising, in part, a counter wherein the counter is a counter for delivering the count value by counting the number of the effective transition edges of the output clock signal, existing during the counting period when the reference clock signal is at a High level, and the counter, the subtracter, the control voltage generation circuit, and the voltage control oscillator circuit having response characteristics such that when the count value is changed from a preceding count value, the frequency of the output clock signal is changed during a period in which the reference clock signal is a Low level, after the end of the counting period and before the start of a succeeding counting period. Applicant respectfully submits that the Kokubo et al. patent does not disclose or suggest the clock multiplication circuit as claimed in the present invention.

Particularly, the clock multiplication circuit of independent claim1 relates to Figure 3 in the Specification and recites, in part, that the counter is a counter for delivering the count value by counting the number of the effective transition edges of the output clock signal, existing

during the counting period when the reference clock signal is at a High level. The Kokubo et al. patent, however, as shown in Fig. 4, discloses a counting period defined by "both a High level and a Low level" as one cycle is shown.

More particularly, the Kokubo et al. patent, as shown in Fig. 4, discloses a single counting period corresponding to a combination of a single High level period and a single Low level period of the input clock signal fref based on an internal gate signal (B) being generated at the timing when fref (A) transits from High to Low and a counter counting 1 to Nv during the Low and High period. Furthermore, the Kokubo et al. patent fails to disclose the response characteristics of DAC9, LPF4 and VCO1. Accordingly, there is no disclosure of when the frequency of fout varies.

With respect to the clock multiplication circuit as claimed in independent claim 1, it, however, recites that a single counting period corresponds to a single High level period of the reference clock signal as well as having response characteristics. Accordingly, the frequency of the output clock signal varies during a Low level period up to the start of a succeeding High level period which is the next counting period. Based on such structure, the output clock signal can therefore be controlled per one cycle of the reference clock signal so that jitter can be reduced and can produce earlier stabilization of the frequency. The clock multiplier of the Kokubo et al. patent does not disclose or suggest such a clock multiplication circuit, as claimed.

With respect to newly added independent claim 23, the clock multiplication circuit of this claim relates to Figure 4 in the Specification and recites, in part, that the counter is a counter for delivering the count value by counting the number of the effective transition edges of the output clock signal, existing during the counting period when the reference clock signal is at a Low level as well as having response characteristics. As discussed, the Kokubo et al. patent merely

discloses a counting period defined by "both a High level and a Low level" as one cycle. In view of this and the distinctions above, such therefore does not disclose or suggest the clock multiplication circuit, as claimed in independent claim 23.

With respect to amended independent claim 3, the clock multiplication circuit of this claim relates to Figures 5 and 7 of the Specification and recites, in part, that the counter is a counter for obtaining the count value at the end of each High level period and each Low level period of the reference clock signal, and the counter, the subtracter, the control voltage generation circuit and the voltage control oscillator circuit having response characteristics in which when the count value obtained by counting during a certain High level period is changed from a preceding count value, the frequency of the output clock signal is changed from the end of the High level period to the start of the next High level period and the characteristics in which when the count value obtained by counting during a certain Low level period is changed from a preceding count value, the frequency of the output clock signal is changed after end of the Low level period and before the start of the succeeding Low level period. More particularly, a counter is obtained at the end of each High level period and each Low level period. Accordingly, the frequency of the output clock signal can be controlled twice per one cycle of the reference clock signal. This means that control is executed twice as much as compared to the disclosure of Figure 4 of the Kokubo et al. patent. Accordingly, unlike the clock multiplier of Kokubo et al., the clock multiplication circuit of independent claim 3 allows for the earlier reduction of jitter as well as stable performance control. Furthermore, the clock multiplication circuit of independent claim 3 allows for the changing of the response of the frequency of the output clock signal which is not disclosed or suggested by Kokubo et al. Based upon the above, it is submitted the Kobuko et al. patent does not disclose or suggest the clock multiplication circuit of independent claim 3.

With respect to amended independent claim 5, the clock multiplication circuit of this claim relates to Figures 3, 4 and 5 of the Specification and recites, in part, a subtracter delivering a difference value in sync with the output clock signal generated after the counter generates the count value and a control voltage generation circuit generating an analog control signal in sync with the output clock signal generated after the subtracter generates the difference value. In the Kokubo et al. patent, as shown in Figure 4, the operation of the comparator (D1, D2) and the corresponding operation of the register vary at the timing of generation of the internal gate signal (B), not in sync with the output clock signal. As shown in Figure 2 of Kokubo et al., the input clock signal (fref) is not input to the comparator 7 and the register 8. Accordingly, the Kokubo et al. patent does not disclose or suggest the clock multiplication circuit of independent claim 5.

With respect to amended independent claim 6, the clock multiplication circuit of this claim relates to Figure 7 of the Specification and recites, in part, that the counter counts each rising edge at which the output clock signal transits from a Low level to a High level and each falling edge at which the output signal transits from the High level to the Low level as the effective transition edges of the output clock signal.

It is noted that with respect to this claim, the Examiner states that "[t]he counter counts the frequency of the output clock (fout) that includes low and high level or in other words, including falling/rising edges." However, in Kokubo et al., at col. 3, ls. 14-18, it states "[r]eferring again to FIG. 2, the counter 5 counts cycles of the output clock signal (fout) during each cycle of the input clock signal (fref). It will be assumed below that the counter 5 counts the falling transitions of fout from each falling transition of fref to the next falling transition of fref." In Kokubo, as above, the counter 5 counts the falling transitions (corresponding to the falling edge in the present invention) of the output fout of VCO. The Kokubo et al. patent has no

disclosure about counting the rising edge. Accordingly, the clock multiplication circuit of the present invention can reduce jitter of the frequency of an allowable output clock signal as the effective transition edge to about half as compared with the case where one edge (i.e., a rising edge or falling edge) is used. Accordingly, the Kokubo et al. patent does not disclose or suggest the clock multiplication circuit of claim 6.

With respect to independent claim 7, it is directed to Figures 8 to 10 and recites, in part, that a multiplier is provided between a subtracter and a control voltage generation circuit. Claims 8 to 10 depend on claim 7. In the Office Action, the Examiner notes that the controller 10 and the accumulator register 18 in combination correspond to a multiplier and further the accumulator register 18 corresponds to a shift register. However, in Kokubo et al., at col. 7, ls. 4-11, there is no disclosure showing such structure. Rather according to Kokubo et al., the accumulator register 18 is to add the difference and has no function of shifting a bit, as with the shift register, to multiply a value by a predetermined factor which is the 'n'th, such as second and half, power of 2. Accordingly, the Kokubo et al. patent does not disclose or suggest the clock multiplication circuit, as claimed in claim 7.

The Examiner also rejected claim 10 based on the disclosure of Kobuko et al., at Figure 8 and col. 3, ls. 60-64. However, Figure 8 merely shows switching of the characteristics of a lowpass filter 4 (see col. 6, ls. 33-38). The disclosure in col. 3, ls. 60-64 on the other hand, relates to initialization of the register 8 by the controller 10 before the start of operation which is unrelated to Figure 8. Further, a lock-in period as claimed in claim 10 is unrelated to initialization. Accordingly, it is submitted that the Kokubo et al. patent does not disclose or suggest the clock multiplication circuit, as claimed in claim 10.

With respect to claims 11 and 12, they are directed to Figures 11-14 and Figures 13-14, respectively. In the Office Action, however, the Examiner states that the disclosure of Kokubo et al., discloses claim 11 at col. 7, ls. 22-29. However, this disclosure in Kokubo et al., discloses that the fourth embodiment referring to Figure 11 is effective when the input clock signal has a low frequency and the value of N is large, but has no disclosure about switching the reference value N. Indeed, switching from a first feedback loop to a second feedback loop indicates that the switching from a path using the subtracter 17 and others to a path using the phase detector 3 by turning off SW1 and turning on SW2. Such is unrelated to the value N. This is shown in Kokubo et al., at col. 3, ls. 5-57. Accordingly, it is submitted that the Kokubo et al. patent does not disclose or suggest the clock multiplication circuit, as claimed in claim 11.

With respect to claim 12, the Examiner relies on the disclosure at col. 3, ls. 23-25 in Kokubo et al. However, this disclosure shows that a memory device 6 stores a predetermined value N and is not configured to externally store a reference value N. Accordingly, there is no disclosure for externally storing the reference value N. Accordingly, it is submitted that the Kokubo et al. patent does not disclose or suggest the clock multiplication circuit, as claimed in claim 12.

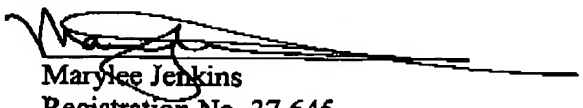
Based upon the forgoing, Applicant respectfully submits that each and every element recited within the independent claims are neither disclosed nor suggested by the Kokubo et al. patent, and are therefore patentable and in condition for allowance. Reconsideration is requested. It is further submitted that the dependent claims are also patentable and in condition for allowance due to their dependency upon the independent claims, since the dependent claims differ in scope from the corresponding parent claims and thus are further limited to additional features of the invention. Therefore, it is respectfully submitted that the dependent claims are

patentable over the Kokubo et al. patent for at least the reasons set forth above with respect to the independent claims. Reconsideration is requested.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicant's undersigned counsel at the telephone number, indicated below, to arrange for an interview to expedite the disposition of this application.

Dated: November 10, 2005

Respectfully submitted,



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